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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/974,721	10/09/2001	Jian Zhou	M-11928 US	7841
34036	7590	05/03/2006	EXAMINER	
SILICON VALLEY PATENT GROUP LLP 2350 MISSION COLLEGE BOULEVARD SUITE 360 SANTA CLARA, CA 95054			LAROSE, COLIN M	
			ART UNIT	PAPER NUMBER
			2624	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/974,721	ZHOU ET AL.	
	Examiner	Art Unit	
	Colin M. LaRose	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 22 March 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-16, 22, 24 and 25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 9-16 is/are allowed.
- 6) Claim(s) 1-8, 22 and 25 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Arguments and Amendments

1. Applicant's amendments and arguments filed 22 March 2006, have been entered and made of record.

Response to Amendments and Arguments

2. Applicant's remarks regarding the § 102(b) rejection of claim 1 in view of Hennessey have been considered but are not persuasive. Applicant asserts that Hennessey does not teach that the first and second patterns are at a de-skew site or saving the first and second patterns in a recipe for de-skewing wafers (see Remarks, p. 5). Applicant argues that "de-skewing wafers" and "measuring the amount of misregistration between two layers on a wafer" are fundamentally different processes.

The claim recites, "[a] method for forming a recipe for de-skewing wafers." Examiner construes this preamble as denoting an intended use of the recipe formed by the method -- the intended use being "de-skewing wafers."

Applicant asserts, "de-skewing" refers to "a method of correcting the offset of the position of a wafer that is loaded onto a stage" (see Remarks, p. 5). However, the Specification defines de-skewing as "a method to correct the offset[s] in the coordinates of a location on the wafer where measurements are taken due to repeated loading onto a stage]" (see Specification, paragraph [0005]).

Based on the definition of "de-skewing" presented in the Specification, Examiner construes the term "de-skewing" as encompassing any process that corrects the offset in the

coordinates of a location on a wafer that has been loaded onto a stage. Two examples of de-skewing are:

- (1) a de-skewing process that occurs when a wafer is initially loaded onto a stage, and there is a misalignment between the wafer and a fixed coordinate system by which measurements are taken -- the wafers is moved relative to the coordinate system to compensate for the misalignment; (this process is disclosed by Hennessey in figure 4);
- (2) a de-skewing process that aligns individual wafer layers to each other; that is, corresponding fixed coordinate locations of subsequent wafer layers may be offset (i.e. misaligned) from previous ones, so in order to compensate for such an offset, it is desirable to "de-skew" the wafer for those layers. In this context, the wafer can be de-skewed so that subsequent wafer layers of the same lot can be formed in perfect alignment; (this process is disclosed by Hennessey in figures 9-12).

See also Hennessey, column 10/29-52.

The claim merely calls for the recipe to have an intended use of "de-skewing wafers," which Hennessey is considered to disclose. Hennessey teaches determining the misalignment between wafer layers in figure 11. Hennessey then uses the determined misregistration to in order to compensate for the misregistration (i.e. to correct the offset between the layers). See columns 9/31-45 and 10/13-20. Such a process of compensating for the offset is considered the same as "de-skewing" the wafer during the etching of wafer layers. As such, Hennessey is considered to disclose de-skew sites and saving the first and second paterns in a recipe for de-skewing wafers, as claimed.

3. Applicant's remarks regarding the § 102(e) rejection of claim 1 in view of Michael have been considered but are not persuasive. Applicant asserts (1) that figure 14 of Michael "is not related to 'forming a recipe for de-skewing wafers,'" and (2) that "Michael does not disclose 'learning a first pattern at a de-skew site on a first wafer layer' and 'learning a second pattern at the de-skew site on a second wafer layer'" (see Remarks, p. 6).

Regarding the first assertion, Michael's figure 14 is considered to be "related" to forming a recipe for de-skewing wafers insofar as it details the process of determining the "relative displacement" between the 1-D template image (corresponding to the first pattern) and the 1-D feature image (corresponding to the second pattern). Such relative displacement is subsequently incorporated into a "recipe," or method, for de-skewing wafers during a photo-etching process or the like. See column 9/52-64: the translational and rotational offsets are used in a method for "adjusting the stepper position to achieve registration of the mask with respect to pre-existing patterns on the wafer."

Regarding the second assertion, Michael is considered to learn both a first and second pattern on different wafers layers. The first pattern corresponds to the pattern extracted from a "good sample" via the process of figure 11 into a 1-D template image. The second pattern corresponds to the pattern extracted from a run-time sample via the process of figure 14 into a 1-D feature image. Both of these patterns are in different layers -- the first pattern is learned from a reference sample, and the second pattern is learned from a run-time sample where the pattern may have been degraded in some way by any of the process steps for forming the pattern.

4. Regarding claim 22, the current amendments are sufficient to overcome the § 102(b) rejection thereof in view of Hennessey. However, the claim has been rendered indefinite for the reasons cited below.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 4-6, 22, and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 22 calls for a comparison of "the first pattern to the de-skew site on the first wafer layer" and a comparison of "the first pattern to the de-skew site on the second wafer layer."

It is unclear how "patterns" are compared to "de-skew sites." Paragraph [0056] of the Specification states that in process step 408 of figure 4, "a search * * * is performed by comparing patterns on the wafer layer with the learned patterns in the recipe." (emphasis added)

Therefore, it appears that the Specification teaches that the first pattern ("learned pattern") is compared to patterns on the wafer layer, rather than a de-skew site on the wafer layer. The search is performed in order to locate a de-skew site, however, it appears that the search is carried out by ascertaining where a pattern that corresponds to the de-skew site is located.

Correction and/or clarification of this discrepancy are required.

Likewise, claim 4 calls for comparing "the first pattern to the de-skew site." Correction and/or clarification of the aforementioned discrepancy are required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,696,835 by Hennessey et al. ("Hennessey").

Regarding claim 1, Hennessey discloses a method (figures 9-12) for forming a recipe for de-skewing wafers, comprising:

learning a first pattern at a de-skew site on a first wafer layer (step 174, figure 11: method learns a first target pattern on a first layer via conversion to a first target primitive);

saving the first pattern and its location in a recipe for de-skewing wafers (i.e. the first target primitive and its designated location are somehow saved so that they can later be utilized for comparison to a second target primitive at step 176 – see e.g. figure 12);

learning a second pattern at the de-skew site on a second wafer layer (step 174, figure 11: method learns a second target pattern on a second layer via conversion to a second target primitive); and

saving the second pattern in the same recipe for de-skewing wafers (i.e. the second target primitive and its designated location are somehow saved so that they can later be utilized for comparison to the first target primitive at step 176 – see e.g. figure 12).

Regarding claim 24, Hennessey teaches that the first wafer layer is a top surface of said wafer and said second wafer layer is the top surface of said wafer after said wafer is processed (figures 10 & 12; col. 9/46-52: both of the first and second targets 158/160 are on the top surface of the wafer after the processing of their respective layers, as shown in figures 10 and 12).

9. Claim 1 is rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent 6,240,218 by Michael et al. (“Michael”).

Regarding claim 1, Michael discloses a method (figures 11 and 14) for forming a recipe for de-skewing wafers, comprising:

learning a first pattern at a de-skew site on a first wafer layer (figure 11 details the process of learning a template pattern on a wafer to generate a 1-D template image; the template pattern is a “good” sample located at a de-skew site (i.e. an area containing a fiducial mark) in a wafer layer, and learning the template pattern comprises generating a 1-D projection thereof – see e.g. column 7, lines 6-13);

saving the first pattern and its location in a recipe for de-skewing wafers (i.e. the projection of the template pattern is somehow saved so that it can later be utilized during the run-time phase for comparison to a 1-D feature image at step 158, figure 14; included with the projection of the template pattern is information regarding its location, or origin – see column 7, lines 14-25);

learning a second pattern at the de-skew site on a second wafer layer (figure 14 details the process of learning a feature pattern on a wafer to generate a 1-D feature image at step 156; the feature pattern is located at the de-skew site in a different wafer layer, such as any of the subsequent layers depicted in figure 1, and learning the feature pattern comprises generating a 1-D projection thereof – see e.g. column 8, lines 30-37); and

saving the second pattern in the same recipe for de-skewing wafers (i.e. the projection of the reference pattern is somehow saved so that it can later be utilized for comparison to the 1-D template image at step 158, figure 14).

It should be noted that Michael does not expressly disclose saving the first and second pattern in a physical medium, such as a memory or the like, however, the claim does not require this. Implicit in Michael's disclosure is that once the projections of the first and second patterns are learned, or extracted, they are retained so that they can be compared to each other. Since the information pertaining to neither pattern is discarded prior to comparison, both learned patterns are both considered to have been "saved," in accordance with the claim language.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 2, 3, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,240,218 by Michael et al. (“Michael”) in view of U.S. Patent 6,240,208 by Garakani et al. (“Garakani”).

Regarding claim 2, Michael does not disclose learning the first pattern comprises determining a score of uniqueness for the first pattern.

Garakani discloses a method for identifying reference patterns to be utilized for aligning wafers. In particular, Garakani discloses that it is advantageous to select reference patterns that are unique. Garakani teaches determining the uniqueness of potential reference patterns, and selecting from among the reference patterns on the basis of their uniqueness scores. For example, in figure 2, the uniqueness of various reference patterns is measured at step 240, and the suggested reference patterns are ordered at step 260 based in part on the uniqueness scores.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Michael by Garakani to determine a score of uniqueness for the first pattern to be learned, since Garakani discloses that it is advantageous to select a reference pattern utilized for aligning semiconductor wafer layers that is unique, and determining a score of uniqueness indicates whether a pattern to be learned is unique (see e.g. column 1, lines 19-32; column 6, lines 58-67).

Regarding claim 3, Garakani discloses selecting a first pattern that has a parameter value (e.g. uniqueness) greater than a threshold (see column 7, lines 51-59). Therefore, that pattern that is learned and saved according to Michael's teachings is sufficiently unique.

Regarding claim 7, Michael discloses learning the first pattern comprises removing a feature of the first pattern (column 7, lines 25-30: "confusing information" within the pattern is deleted).

However, Michael does not disclose determining a score of uniqueness for the first pattern without the feature, and then saving the pattern without the feature when the uniqueness score exceeds a threshold, as claimed.

Garakani discloses a method for identifying reference patterns to be utilized for aligning wafers. In particular, Garakani discloses that it is advantageous to select reference patterns that are unique. Garakani teaches determining the uniqueness of potential reference patterns, and selecting from among the reference patterns on the basis of their uniqueness scores. For example, in figure 2, the uniqueness of various reference patterns is measured at step 240, and the suggested reference patterns are ordered at step 260 based in part on the uniqueness scores.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Michael by Garakani to determine a score of uniqueness for the first pattern to be learned, since Garakani discloses that it is advantageous to select a reference pattern utilized for aligning semiconductor wafer layers that is unique, and determining a score of uniqueness indicates whether a pattern to be learned is unique (see e.g. column 1, lines 19-32; column 6, lines 58-67). Furthermore, it would have been obvious to compute the uniqueness score of the pattern and save the pattern with portions thereof deleted, since Michael teaches that it is

advantageous to remove extraneous features within the pattern that do not relate to the salient features and are simply “confusing” (Michael, column 7, lines 25-30).

13. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,240,218 by Michael et al. (“Michael”), as applied to claim 1 above, in view of U.S. Patent 6,681,151 by Weinzimmer et al. (“Weinzimmer”).

Regarding claim 8, Michael does not disclose that saving the first pattern in the recipe comprises saving a file name of a file including the first pattern. However, at the time of the invention, it was well-known in the art to store captured image data into image files. More particularly, Weinzimmer shows that it was obvious to store extracted fiducial patterns into data files for later use (see column 10, lines 35-53). Such a method of saving extracted fiducial data in a file is advantageous in that the file is easily accessible for future and/or repeated use.

Allowable Subject Matter

14. Regarding claim 9, Michael discloses the learning and saving steps, as noted above for claim 1. However, Michael does not appear to disclose the step of “dividing,” as claimed.

Michael’s disclosure focuses on the problem that patterns to be detected in subsequent wafer layers (cf. figure 18) may be degraded to point where they are indistinguishable from background. See column 1, lines 33-52.

Michael’s disclosure proposes a solution to this problem and is illustrated in figure 7. In figure 7A, a 1-D projection of a “good” pattern consists of three discernible spikes. Figure 7B shows a degraded pattern to be matched to the good pattern. Two of the degraded pattern’s

spikes have been attenuated, while the third spike is missing (i.e. indistinguishable from background noise). Michael's system is able to recognize the degraded pattern even though it contains missing features.

Claim 9 seeks to remedy the same problem but does so in a different way. Michael does not disclose "diving additional wafer layers into a plurality of layers where the de-skew site can be recognized using the first pattern and at least one wafer layer where the de-skew site cannot be recognized using said pattern." In contrast, Michael does not divide out layers whose patterns are substantially degraded to the point that they cannot be recognized, because Michael teaches that they can be recognized using a 1-D projection even when they are severely degraded. Since Michael purports that all of the degraded patterns can be recognized, there is no disclosure of separating layers where the de-skew site can be recognized from those in which it cannot be recognized.

In addition, Michael does not disclose the learning and saving of an additional pattern for recognition of the "cannot be recognized" pattern(s), since none of Michael's de-skew site are unable to be recognized.

For these reasons, claims 9-16 are allowable.

15. Claims 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and to overcome the above rejection under § 112, 2nd paragraph.

Regarding claim 4, neither Hennessey nor Michael fairly discloses or suggests comparing the first pattern to the de-skew site on the second wafer layer before said learning the second

pattern. In both Hennessey and Michael, the patterns are compared after both patterns have been learned.

16. Claims 22 and 25 would be allowable if rewritten to overcome the above rejection under § 112, 2nd paragraph.

Regarding claim 22, Hennessey does not fairly teach or disclose using the learned first pattern to de-skew a wafer by comparing it to the de-skew site on the first layer, and then comparing it to the de-skew site on the second layer when the first pattern matches the second pattern, as claimed.

Related Prior Art

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,898, 306 by Lu.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

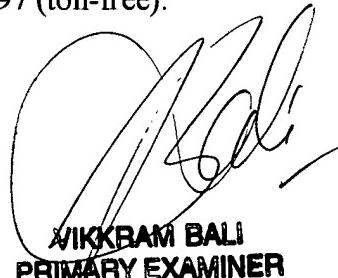
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the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colin M. LaRose whose telephone number is (571) 272-7423. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jingge Wu, can be reached on (571) 272-7429. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2600 Customer Service Office whose telephone number is (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CML
Group Art Unit 2624
26 April 2006



VIKKRAM BALI
PRIMARY EXAMINER